CLAIMS

Sub a1

1. A semiconductor device having a plurality of resistor elements formed on an insulating film in predetermined regions on a surface of a semiconductor substrate, said semiconductor device comprising active regions contiguous with said resistor elements.

2. A semiconductor device according to claim 1, wherein said insulating film is element isolating film formed by shallow trench isolation.

3. A semiconductor device according to claim 1, wherein said plurality of resistor elements are arranged on said insulating film and wherein said insulating film under said resistor elements is set to a predetermined width by said active regions.

Sub a2

4. A semiconductor device according to claim 3, wherein said predetermined width is defined by an amount of shift in resistance value of said resistor elements, said amount of shift being defined by said predetermined width.

5. A semiconductor device according to claim 1, wherein the regions including said active regions are furnished with dummy gate electrodes constituting the same layer as that of said resistor elements.

6. A semiconductor device according to claim 5, wherein said dummy gate electrodes are wider in area than

said active regions which are covered entirely with said dummy gate electrodes.

7. A semiconductor device according to claim 5, wherein each of said active regions is furnished with a plurality of said dummy gate electrodes.

8. A semiconductor device according to claim 5, wherein a distance between each of said resistor elements and each of said dummy gate electrodes is held constant.

9. A semiconductor device according to claim 1, wherein a plurality of said resistor elements are furnished between any adjacent two of said active regions.

10. A semiconductor device according to claim 9, wherein a distance between any adjacent two of said plurality of said resistor elements is set to a minimum space between patterns formed by conductive film constituting the same layer as that of said resistor elements on said semiconductor substrate.

11. A semiconductor device according claim 1, wherein said active regions extend close to lengthwise ends of said resistor elements which are surrounded by said active regions.

12. A semiconductor device according to claim 5, wherein said dummy gate electrodes extend close to lengthwise ends of said resistor elements which are surrounded by said dummy gate electrodes.

13. A semiconductor device according to claim 1, wherein said resistor elements are formed by a layer constituting gate electrodes of MOS transistors furnished outside said predetermined regions.

14. A method of manufacturing a semiconductor device comprising the steps of:

firstly performing etching to remove surroundings of a plurality of parallelly arranged strip-shaped rectangular regions in predetermined regions on a semiconductor substrate in order to have trenches formed by the rectangular regions left intact;

secondly filling said trenches with insulating film formed on said semiconductor substrate;

thirdly polishing surfaces of said insulating film for removal thereof from regions except those of said trenches, thereby establishing said rectangular regions as active regions and planarizing the surfaces of said insulating film on said trenches;

fourthly forming on said semiconductor substrate conductive film using a material having a predetermined resistance value; and

fifthly patterning said conductive film on said insulating film so as to form rectangular resistor elements extending between any adjacent two of said active regions and in parallel with said active regions.

15. A method of manufacturing a semiconductor device according to claim 14, wherein a distance between any adjacent two of said active regions is determined by a permissible range of resistance values of said resistor elements formed in said fifth step.

16. A method of manufacturing a semiconductor device according to claim 14, wherein said fifth steps produces dummy gate electrodes together with said resistor elements in regions including said active regions, said dummy gate electrodes being made of said conductive film and extending substantially in parallel with said resistor elements.

17. A method of manufacturing a semiconductor device according to claim 14, wherein said fifth step produces said resistor elements while forming dummy gate electrodes which extend from said active regions onto said insulating film and which surround said resistor elements.

18. A method of manufacturing a semiconductor device according to claim 14, wherein said fifth step produces said resistor elements while patterning gate electrodes of MOS transistors formed by said conductive film outside said predetermined regions.

19. A method of manufacturing a semiconductor device according to claim 16, wherein a distance between each of said resistor elements and each of said dummy gate electrodes is set to a minimum space between patterns

formed by said conductive film on said semiconductor substrate.

20. A method of manufacturing a semiconductor device according to claim 16, wherein said dummy gate electrodes are formed so as to cover entirely said active regions.

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